REMARKS

This amendment is in response to the Office Action dated 5/12/04. Entry of this Amendment and reconsideration of this application are respectfully requested.

Claim Objections

Claim 43 was objected to under 35 CFR §1.75(c). Claim 43 has been cancelled.

Claim Rejections under 35 USC §112

Claims 14-16 and 36 were rejected as indefinite under 35 USC §112.

In response:

- claim 14 has been amended so that the step of "preconditioning" is properly introduced in claim 14, thereby overcoming the insufficient antecedent basis problem cited by the Examiner;
- claim 15 has been amended to eliminate the redundancy cited by the Examiner;
- claim 16 has been amended so that a driving stage is properly introduced in claim 16, thereby overcoming the insufficient antecedent basis problem cited by the Examiner; and
- claim 36 has been amended to eliminate any reference to a "keep alive transistor", and to explicitly specify the connections for the claim's "bleed resistor" element.

It is believed that these amendments overcome all the §112 claim rejections.

Rewritten in Independent Form

With the exception of the §112 rejections discussed above (and which should now be overcome), no substantive objections or rejections were noted for dependent claims 14-21, 37 and 38,

thereby indicating that these claims would be allowable if rewritten in independent form incorporating all the limitations of their base claims and any intervening claims.

Accordingly, claims 14, 16 and 21 have been rewritten in independent form, incorporating all the limitations of their base claim (claim 1) and any intervening claims (none). Claim 37 was rewritten in independent form, incorporating all the limitations of its base claim (claim 24) and any intervening claims (none).

The rewritten claim 14 is the parent of claim 15, the rewritten claim 16 is the parent of claims 17-20, and the rewritten claim 37 is the parent of claims 38. Therefore, each of claims 14-21, 37 and 38 should now be in proper form for allowance.

Please note that a number of amendments have been made to claims 14-21, 37 and 38, in addition to the basic "rewriting" noted above. These additional amendments were made to overcome rejections under §112, or to otherwise clarify the claim language and to more particularly point out the subject matter which the applicant regards as the invention.

Please also note that rewriting dependent claims 14, 16 and 21 in independent form are amendments purely of form, since they do not introduce any new limitations into the dependent claims.

Claim Rejections under 35 USC §102

Claims 1-2, 4-5, 8-13, 22-30, 32-33, 36 and 39-43 were rejected under 35 USC §102(b) as anticipated by a patent to Schuler et al.

Claim 1

Claim 1 has been amended to better clarify and more particularly point out the subject matter which the applicant regards as his invention. Claim 1 is directed to a method for

improving high-speed output buffer components. As amended, the recited method comprises:

- establishing a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals;

- establishing a differential pair module comprising two transistors, each of which has a control input and first and second current terminals;

- the cascode module connected to receive at its second current terminals a substantially differential current signal from the first terminals of the differential pair module and to transmit at its first current terminals the substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform; and

- engineering the resistive loads seen by the first terminals of the differential pair module, based on one or more criteria thereby engineering the symmetry between the rising edge and the falling edge for each of the first output waveform and the second output waveform.

As amended, claim 1 recites a specific relationship between its differential pair module, its cascode module, the external load impedances, and the resistive loads that are engineered. Specifically, the transistors of claim 1's cascode module are required to be in a cascode relationship with the transistors of the differential pair module - i.e., the cascode transistors are connected in series with the differential pair module transistors such that the transistors of the cascode module conduct the differential pair module's substantially differential current signal to the external load impedances.

Examples of this arrangement are shown in FIGs. 1A-1D and

FIG. 2. In FIG. 1A, for example, transistors 150 and 160 form a differential pair module 140, transistors 130 and 135 form a cascode module 120, and resistors 110 and 115 form resistive loads 100. The currents conducted by differential pair module transistors 150 and 160 are conducted by resistive loads 100 and cascode module transistors 130 and 135 to output terminals OUTP and OUTN, to which the external load impedances are connected.

The recited structure is essential to the proper operation of the invention, and to achieving the stated goal of engineering the symmetry between the rising and falling edges for the first and second output waveforms. By definition, a "cascode transistor" is connected in series with a "primary" transistor - i.e., with its emitter connected to the primary transistor's collector (for a bipolar implementation) or its source connected to the primary transistor's drain (for a FET implementation) - such that the cascode transistor conducts the primary transistor's current. When a pair of transistors are cascoded with the transistors of a differential pair, the characteristics of the cascode pair affect the resistance at the collector nodes of the differential pair (assuming a bipolar implementation), minimizes the effect of Miller capacitance, and provides good isolation between the differential pair and the output nodes. Thus, connecting a cascode module between the differential pair and the buffer's output nodes - as required by claim 1 - serves to enable the circuit designer to engineer the symmetry between the rising and falling edges for the first and second output waveforms using the techniques described in the present application. Without the isolating cascode module, the differential pair's first current terminals would connect to the external load impedances; as such, the impedance seen by the differential pair would be controlled by the value of the external load impedances, thus preventing an optimization of this

value. Moreover, the voltages at the junctions with the external loads could further affect the capacitances between the control and first current terminals of the differential pair transistors, leading to a highly undesirable dependence of the output waveform symmetry on an external termination voltage that users may generally want to optimize for other system goals.

The circuitry disclosed in the cited patent to Schuler is completely different. Schuler's circuit is designed to dampen overshoot and undershoot for signals applied to the write head of a disc drive. Schuler does not discuss using his circuit as a high-speed output buffer, and says nothing about controlling the symmetry between the rising and falling edges of his output waveforms. Schuler discloses a differential pair module, but that is all his design has in common with the claimed invention: it is entirely different from the claimed invention both structurally and functionally.

The Examiner attempts to correlate the elements of claim 1 with components shown in Schuler's FIG. 2, but under careful examination, most of these correlations are seen to be non-existent. For example, the Examiner identifies Schuler's Q9 and Q10 as corresponding to the "cascode transistor module" of claim 1. This is incorrect. Schuler's Q9 and Q10 do not form a cascode module. As noted above, a cascode transistor is connected in series with a primary transistor such that the cascode transistor conducts the primary transistor's current. Schuler's Q9 and Q10 transistors do not form a cascode module. These transistors are not connected in cascode fashion, and neither provides the functionality required of a cascode transistor. Rather, Q9 and Q10 act as simple current switches, controlled by switch S3, which affect the currents at nodes N1 and N2: when S3 is connected to VCC, Q9 and Q10 are off and conduct no current; alternatively, when S3 is connected to V3, Q9 and Q10 conduct a

current having a value that depends on the value of V3. Thus, Schuler fails to disclose either the structure of or the function provided by the "cascode transistor module" of the amended claim 1.

Claim 1 also requires the cascode transistor module transmit at its first current terminals the substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform. Thus, claim 1 requires that the substantially differential current signal be received on one side of the cascode transistors (their "second terminals - e.g., their emitters) and be transmitted to the cascode transistors' other side (their "first terminals - e.g., their collectors). Schuler discloses nothing analogous to this. Even if Schuler's Q9 and Q10 did form a cascode module, Q9 and Q10 do not conduct the differential pair currents from one side of the cascode to the other, or to any external load impedances - the currents conducted by Q9 and Q10 are simply conducted to supply voltage Vee.

Furthermore, the outputs of Schuler's "cascode" transistors Q9 and Q10 are taken at their emitters - i.e., the same terminals as those coupled to his differential pair transistors - not the opposite terminals as required by claim 1.

Thus, the Schuler circuit differs from that recited in the amended claim 1 in virtually every respect. Schuler's circuit:

- lacks a cascode transistor module as required by the amended claim 1;

- does not transmit the differential pair currents to any external load impedances in the manner required by claim 1;

- does not produce first and second output waveforms as recited in claim 1; and

- discloses no means by which the symmetry between the rising and falling edges for the first and second output

waveforms may be engineered.

Schuler discloses a programmable damping circuit, while the applicant has invented and claimed a high speed output buffer for which the symmetry between the rising and falling edges for the first and second output waveforms can be engineered. The two circuits are designed for completely different purposes, and have completely different topologies and methods of operation. As noted above, virtually none of the elements of the amended claim 1 are disclosed in Schuler. Therefore, Schuler cannot and does not anticipate the amended claim 1. The amended claim 1 is thus allowable over Schuler.

The amended claim 1 is the parent of each of claim 2, 4-5, 8-13 and 22-23, each of which is therefore allowable along with claim 1. It should be noted, however, that many of these claims are patentably distinct from Schuler, and are thus allowable on independent grounds.

Claims 2 and 4 identify particular transistors as bipolar, but also provides additional details regarding the structure of the circuitry recited in the amended claim 1. Though Schuler discloses some bipolar transistors, he does not disclose the structures specified in claims 2 and 4, which are therefore allowable on this independent basis.

As the limitation formerly found in claim 5 has been largely incorporated into claim 1, claim 5 has been cancelled.

Claims 8-13 are largely concerned with the "resistive loads" recited in claim 1. Schuler says nothing remotely resembling the subject matter of these claims:

- claims 8-10 specify that the resistive loads are connected

"between said cascode transistor module and said differential pair module such that said resistive module conducts said substantially differential current signal." As noted above, Schuler's Q9 and Q10 do not conduct the substantially differential current signal, and neither do his resistors R5 and R6.

- claim 11 requires that "engineering the resistive loads comprises the step of selecting a cascode bias voltage for said cascode transistor module." When read in combination with parent claim 1, this means that a cascode bias voltage is selected to achieve the goal stated in claim 1 - i.e., "engineering the symmetry between the rising edge and the falling edge for each of said first output waveform and said second output waveform". The Examiner states that switch S3 and voltages V3 and Vcc meet the requirements of claim 11. They do not. Switch S3 simply operates Q9 and Q10 to affect the currents at N1 and N2. Schuler says nothing about engineering the symmetry of any output waveforms, and with Schuler's structure being so completely different from that of the applicant, it is impossible for Schuler to meet the requirements of claim 11.

- similarly, claims 12 and 13 require engineering the resistive loads to achieve very specific goals, none of which are mentioned or achieved by Schuler. Claim 12 recites that engineering the resistive loads requires "selecting resistance values for said loads to obtain a desired range $V_{io,max} - V_{io,min}$, where V_{io} is the voltage between the control input and the first terminal of a differential pair module transistor". Claim 13 recites that engineering the resistive loads requires "selecting a cascode bias voltage to obtain a desired rate of change of C_{io} as a function of V_{io}, where C_{io} is the capacitance between the control input and the first terminal of a differential pair module transistor and V_{io} is the voltage between the control input and

the first terminal of a differential pair module transistor". The Examiner states that these steps are somehow "inherently seen in Fig. 2". They are not. Engineering the resistive loads with the specific goals of claims 12 and 13 in mind is neither disclosed, suggested or shown anywhere in Schuler, nor are these disparate goals in any way "inherent".

Therefore, claims 8-13 are therefore allowable on these independent bases.

Claim 24

Claim 24 is an apparatus claim directed to an improved high-speed output buffer component. Claim 24 has been amended in a manner similar to that of claim 1, to better clarify its differences with respect to the cited art. As amended, claim 24 requires:

- a cascode transistor module comprising two transistors, each of which has a control input and first and second current terminals;

- a differential pair module comprising two transistors, each of which has a control input and first and second current terminals, the cascode transistor module arranged to receive at its second current terminals a substantially differential current signal from the first terminals of the differential pair module and to transmit at its first current terminals the substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform, wherein the cascode transistor module further comprises:

- a resistive load comprising first and second resistances, the first resistance connected between the first terminal of one of the differential pair module transistors and the second terminal of one of the cascode module transistors, and

the second resistance connected between the first terminal of the other of the differential pair module transistors and the second terminal of the other of the cascode module transistors; and

- a cascode bias voltage node for applying a cascode bias voltage to the control inputs of the cascode transistor module transistors, wherein the symmetry between the rising edge and the falling edge for each of the first output waveform and the second output waveform may be altered by careful selection of one or more elements selected from the list of:

the resistive load, and

the cascode bias voltage.

Thus, the amended claim 24 recites a very specific structural relationship between the output buffer's differential pair module, cascode transistor module, external load impedances, and resistive loads. The amended claim clearly and explicitly requires a topology equivalent to those shown in FIGs. 1A-1D and FIG. 2 - with the cascode module transistors and the resistive load connected in series between the differential pair and the external load impedances. None of these relationships are present in the Schuler circuit.

The discussion of the differences between Schuler and the applicant's invention put forth above in relation to claim 1 is also applicable to claim 24. To repeat, Schuler fails to disclose:

- a cascode transistor module connected to receive at its second current terminals a substantially differential current signal from the first terminals of the differential pair;
- a cascode module arranged to transmit at its first current terminals the substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform; and

- a resistive load connected between the cascode module and the differential pair such that it conducts the substantially differential current signal from the first terminals of the differential pair;

all of which are required by the amended claim 24.

As noted above, Schuler's Q9 and Q10 do not form a "cascode transistor module" as asserted by the Examiner. Rather, Q9 and Q10 act as simple current switches, controlled by switch S3, that affect the currents at nodes N1 and N2. Furthermore, Schuler's Q9 and Q10 do not conduct the differential pair currents to any external load impedances - the currents conducted by Q9 and Q10 are simply conducted to supply voltage Vee.

Thus, the Schuler circuit differs from that recited in the amended claim 24 in virtually every aspect. Schuler discloses a programmable damping circuit, while the applicant has invented and claimed a high speed output buffer for which the symmetry between the rising and falling edges for the first and second output waveforms can be engineered. The two circuits are designed for completely different purposes, and have completely different topologies and methods of operation.

As virtually none of the elements of the amended claim 24 are disclosed in Schuler, Schuler cannot and does not anticipate the amended claim 24. The amended claim 24 is thus allowable over Schuler.

The amended claim 24 is the parent of claims 25-30, 32-33, 36 and 39-43, which should therefore be allowable along with claim 24. It should be noted, however, that many of these claims are patentably distinct from Schuler, and are thus allowable on independent grounds.

Claim 29 is similar to claim 12 discussed above. As noted there, Schuler says nothing remotely resembling the subject matter of this claim. Claim 29 requires engineering the cascode bias to achieve a very specific goal, which is never mentioned or suggested by Schuler. Claim 29 requires that the cascode bias voltage is engineered "to obtain a desired range $V_{io,max}$ - $V_{io,min}$, where V_{io} is the voltage between the control input and the first terminal of a differential pair module transistor". The Examiner states that this requirement is somehow "seen to read directly in Fig. 2". It is not. Engineering the cascode bias voltage with the specific goal of claim 29 in mind is neither disclosed, suggested or shown anywhere in Schuler. Claim 29 is therefore allowable on this independent basis.

Claims 30 and 32 identify particular transistors as bipolar, but also provides additional details regarding the structure of the circuitry recited in the amended claim 24. Schuler does not disclose the structures specified in claims 30 and 32, which are thus allowable on this independent basis.

As the limitation formerly found in claim 33 has been largely incorporated into claim 24, claim 33 has been cancelled.

Claim 36 requires that a bleed resistor be "connected between the second current terminals of said cascode transistor module's transistors." A bleed resistor connected as required by claim 36 is not disclosed or suggested in Schuler. It should be noted that the Examiner has not identified an element in Schuler which is said to correspond to the bleed resistor of claim 36. Claim 36 is therefore allowable on this independent basis.

Claim 39 requires that inductive modules be coupled to the "first terminals of said cascode transistor module". If it is accepted that Q9 and Q10 form Schuler's "cascode module", then

its "first terminals" are the collectors of Q9 and Q10. However, as is clearly seen in Schuler's Fig. 2, the collectors of Q9 and Q10 are connected to Vee - not to any inductive modules. The entirely different topology of Schuler's circuit make meeting the requirements of claim 39 impossible. Claim 39 is therefore allowable on this independent basis.

Claim 40 is a dependent claim which has been amended to better clarify its subject matter. As amended, claim 40 is directed to a driving stage which provides a signal input to the control inputs of the transistors of the differential pair module. The driving stage includes a second resistive module connected in series between the driving stage and the control input of one of the differential pair module transistors, and a third resistive module connected in series between the driving stage and the control input of the other differential pair module transistor. The claim further requires that the second and third resistive modules be engineered to obtain a desired symmetry between the rising edge and the falling edge for each of the first output waveform and the second output waveform.

The Examiner identifies resistors R1 and R2 as corresponding to the second and third resistive modules of claim 40. There is no such correspondence. Resistors R1 and R2 are connected in series with the collectors of respective transistors - they are not in series with the bases of respective transistors, as is explicitly required by claim 40. Furthermore, Schuler says nothing about engineering R1 and R2 to achieve desired objectives with respect to the symmetry between the rising edge and the falling edge for each of the first output waveform and the second output waveform, as is also explicitly required by claim 40. In failing to disclose every element of claim 40, Schuler cannot possibly anticipate claim 40. Claim 40 is therefore allowable on this independent basis.

Claim 43 has been cancelled.

Claim Rejections under 35 USC 103(a)

Claims 3, 6-7, 31, 34-35 and 44-45 were rejected as obvious over Schuler.

The amended claim 1 is the parent of claims 3 and 6, which are therefore allowable along with claim 1. However, it should also be noted that claims 3 and 6 identify particular transistors as FETs, and provide additional details regarding the structure of the circuitry recited in the amended claim 1. Schuler discloses neither the use of FETs, nor the structures specified in claims 3 and 6, which are therefore allowable on this independent basis.

Claim 7 has been cancelled.

The amended claim 24 is the parent of claims 31 and 34, which are therefore allowable along with claim 24. However, it should also be noted that claims 31 and 34 identify particular transistors as FETs, and provide additional details regarding the structure of the circuitry recited in the amended claim 24. As noted in connection with claims 3 and 6 above, Schuler does not disclose the use of FETs, or the structures specified in claims 31 and 34, which are therefore allowable on this independent basis.

Claims 35, 44 and 45 have been cancelled.

All of the claims presently in the application are believed to be patentably distinct with respect to the cited art and to otherwise be in proper form for allowance. A Notice of Allowance

is respectfully requested.

Respectfully submitted,

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Steven C. Patrick
Registration No. 40,341
Attorney for Applicant

KOPPEL, JACOBS, PATRICK & HEYBL
555 St. Charles Drive, Suite 107
Thousand Oaks, California 91360
(805)373-0060